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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of
CHIOU-FENG CHEN ET AL.
Serial No. 10/753,103
Filed: January 6, 2004
For: NAND FLASH MEMORY WITH ENHANCED PROGRAM AND ERASE PERFORMANCE, AND FABRICATION PROCESS

Examiner: Johannes P. Mondt
Group Art Unit: 2826
Confirmation No. 2773

July 10, 2006

BRIEF ON APPEAL

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REAL PARTY IN INTEREST

The real party in interest is Silicon Storage Technology, Inc., a California corporation with a place of business in Sunnyvale, California, to whom the application has been assigned.

RELATED APPEALS AND INTERFERENCES

None.

STATUS OF CLAIMS

The application was filed originally with Claims 1 - 23. In an amendment filed October 27, 2005, Claims 14 and 23 were cancelled to minimize filing fees since they had been withdrawn from consideration, Claims 1 - 2, 4 - 6, 8 - 12, 15 - 16, 18 - 20 and 22 were amended, and Claim 24 was added. Claims 1 - 13, 15 - 22 and 24 are on appeal.

Currently, no claims stand allowed.

STATUS OF AMENDMENTS

The only amendment filed since the action from which the appeal is taken is one filed concurrently with this brief for the purpose of correcting minor clerical errors in the specification and in Claims 2 and 3, as well as overcoming a formal rejection which the Examiner had made to Claims 4, 18 and 22.

RELATED APPLICATIONS/PATENTS

None.

SUMMARY OF CLAIMED SUBJECT MATTER

The claims on appeal are directed to a NAND flash memory cell array which, as defined by Claim 1, illustrated in Figures 2 and 7 and described at Page 5, line 6 to Page 6, line 27 and Page 12, lines 1 - 14, comprises a substrate (41) having an active area (52), a bit line diffusion (50) and a source region (51) in the active area with no other diffusions in the active area between the bit line diffusion (50) and the source region (51), a plurality of stacked gates (36) and select gates (43 - 45) arranged alternately in a row above the active area between the bit line diffusion (50) and the source region (51), with each of the stacked gates (36) having a control gate (36) positioned above a floating gate (37) and the last select gate (45) in the row at least partially overlapping the source region (51), a bit line (57) above the row, and a bit line contact (46) interconnecting the bit line (57) and the bit line diffusion (50).

Claims 2 - 13 depend from Claim 1. Claim 2 further specifies that the stacked gates (36) and the select gates (43 - 45) are self-aligned relative to each other.

Claim 3 further calls for a relatively thin tunnel oxide (40) between the floating gates (37) and the substrate (41, 52), a first relatively thick dielectric (47) between the floating gates (37) and the select gates (43 - 45), and a second relatively thick dielectric (42) between the floating gates (37) and the control gates (38).

Claim 4 further specifies that the control gates (38) and the select gates (43 - 45) surround the floating gates (37) in a manner which provides inter-gate capacitances between the select gates (43 - 45) and the floating gates (37) and between the control gates (38) and the floating gates (37) which are large enough to couple voltages between the select gates (43 - 45) and the floating gates (37) and between the control gates (38) and the floating gates (37). See Page 9, lines 8 - 15.

Claim 5 further specifies that erase paths extend from the floating gates (37), through tunnel oxides (40) below the floating gates (37) to channel regions in the substrate (41, 52), and voltage is coupled to the floating gates (37) both from the control gates (38) and from the select gates (43 - 45). See Page 9, line 1 to Page 10, line 2.

Claim 6 specifies that program paths extend from off-gate channel regions between the select gates (43 - 45) and the floating gates (37) to the floating gates (37), and voltage is coupled to the floating gates (37) both from the control gates (38) and from the select gates (43, 45) on the sides of the stacked gates (36) toward the source region (51).

Claim 7 specifies that program paths extend from off-gate channel regions between the select gates (43 - 45) and the floating gates (37) to the floating gates (37), and the select gate (43, 44) on the bit line side of the stacked gates (36) in a selected cell is biased at a lower voltage than the other select gates (43, 45) in the row to control channel current for efficient hot carrier injection during a program operation. See Page 10, lines 8 - 30.

Claim 8 specifies that the select gates (43 - 45) in unselected cells are biased at a voltage to turn on the channels beneath them to form a conduction path between the bit line diffusion and the source region. See Fig. 6.

Claim 9 specifies that the bit line (57) for a row containing a selected cell to be programmed is held at 0 volts, a relatively low positive voltage is applied to a cell select gate (43 - 45) for the selected cell, a relatively high positive voltage is applied to the source region (51) at the end of the row in which the selected cell is located, a relatively high positive voltage is applied to the control gate (38) in the selected cell, a relatively high positive voltage is applied to the select gates (43 - 45) for unselected cells, and a relatively high positive voltage is applied to the control gates (38) in the unselected cells. See Page 10, lines 8 - 17.

Claim 10 specifies that an erase path is formed by a relatively high negative voltage on the control gates (38) and a relatively low negative voltage on the select gates (43 - 45), with the bit line diffusion (50), the source region (51) and the P-well (52) at 0 volts. See Page 9, lines 16 - 20.

Claim 11 wherein an erase path is formed by a relatively high negative voltage on the control gates (38), and relatively low negative voltage on the select gates (43 - 45), with the active area (52) at a positive voltage and the bit line diffusion (50) and the source region (51) floating. See Page 9, lines 20 - 23.

Claim 12 specifies that a read path is formed by turning on the select transistors (43 - 45) and the stacked control and floating gate transistors (38, 37) in unselected cells, with the common source (51) at 0 volts, the bit line diffusion (50) at 1 - 3 volts, and the control gate (38) of the selected cell biased at 0 – 1.5 volts to form a conduction channel under the floating gate (37) for an erase state and a non-conduction channel for a program state. See Fig. 6 and Page 11, lines 18 - 30.

Claim 13 further calls for an erase path which can erase the whole cell array simultaneously and a program path which is single cell selectable. See Page 17, lines 27 - 29.

As defined by Claim 15, illustrated in Figure 7 and described at Page 12, lines 1 - 14, the NAND flash memory cell array comprises a substrate (41) having an active area (52), a bit line diffusion (50) and a source diffusion (51) in the active area with no other diffusions in the active area (52) between the bit line diffusion and the source diffusion, a plurality of stacked gates (36) and select gates (43 - 45) arranged alternately in a row above the active area (52) between the bit line diffusion (50) and the source diffusion (51), with each of the stacked gates (36) having a control gate (38) positioned above a floating gate (37) and the last select gate (45) in the row being directly above the source diffusion (51), a bit line (57) above the row, and a bit line contact (46) interconnecting the bit line (57) and the bit line diffusion (50).

Claims 16 - 18 depend from Claim 15. Claim 16 further specifies that the select gates (43 - 45) are self-aligned to the control and floating gates (38, 37). Claim 17 calls for a relatively thin tunnel oxide (40) between the floating gates (37) and the substrate (41, 52), a first relatively thick dielectric (47) between the floating gates (37) and the select gates (43 - 45), and a second relatively thick dielectric (42) between floating gates (37) and control gates (38). Claim 18 specifies that the control gates (38) and the select gates (43 - 45) surround the floating gates (37) in a manner which provides inter-gate capacitances between the select gates (43 - 45) and the floating gates (37) and between the control gates (38) and the floating gates (37) which are large enough to couple voltages between the select gates (43 - 45) and the floating gates (37) and between the control gates (38) and the floating gates (37). See Page 9, lines 8 - 15.

As defined by Claim 19, illustrated in Figures 2, 4, 7 and 8 and described at Page 5, line 6 to Page 6, line 27 and Page 12, lines 1 - 14, the NAND flash memory cell array comprises a substrate (41) having an active area (42), bit line diffusions (50) and source diffusions (51) spaced alternately in the active area (52) with no other diffusions between them, a plurality of stacked gates (36) and select gates (43 - 45) arranged alternately in rows between the bit line diffusions (50) and the source diffusions (51), with each of the stacked gates (36) having a control gate (38) positioned above a floating gate (37) and the last select gates (45) in each of the rows at least partially overlapping the source diffusions (51) between the rows, a bit line (57) above each row, and bit line contacts (46) interconnecting the bit lines (57) and the bit line diffusions (50).

Claims 20 - 22 depend from Claim 19. Claim 20 further specifies that the select gates (43 - 45) are self-aligned to the control and floating gates (38, 37). Claim 21 calls for a relatively thin tunnel oxide (40) between the floating gates (37) and the substrate (41, 52), a first relatively thick dielectric (47) between the floating gates (37) and the select gates (43 - 45), and a second relatively thick dielectric (42) between floating gates (37) and control gates (38). Claim 22 specifies that the control gates (38) and the select gates (43 - 45) surround the floating gates (37) in a manner which provides inter-gate capacitances between the select gates (43 - 45) and the floating gates (37) and between the control gates (38) and the floating gates (37) which are large enough to couple voltages between the select gates (43 - 45) and the floating gates (37) and between the control gates (38) and the floating gates (37). See Page 9, lines 8 - 15.

As defined by Claim 24, illustrated in Figures 2 and 7 and described at Page 5, line 6 to Page 6, line 27 and Page 12, lines 1 - 14, the NAND flash memory cell array comprises a substrate (41) having an active area (52), a bit line diffusion (50) and a source region (51) in the active area (52) with no other diffusions in the active area between the bit line diffusion (50) and the source region (51), a plurality of stacked gates (36) and select gates (43) arranged alternately in a row above the active area (52) between the bit line diffusion (50) and the source region (51), with each of the stacked gates (36) having a control gate (38) and a floating gate (37) with self-aligned sides adjacent to the select gates (43 - 45), erase paths between the floating gates (37) and channel regions in the active area beneath the stacked gates (36), and voltage coupling from the control gates (38) and the select gates (43 - 45) to the floating gates (37). See Page 9, lines 8 - 12.

GROUNDS OF REJECTION

Claims 19 - 22 have been rejected under 35 U.S.C. §112 as failing to comply with the written disclosure requirement because the Examiner cannot find support in the specification for the limitation calling for bit line diffusions and source diffusions spaced alternately in the active area with no other diffusions between them.

Claims 4, 18 and 22 have been rejected under 35 U.S.C. §112 as being indefinite in claiming an inter-gate capacitance which is large enough for voltage coupling between the gates during program and erase operations.

Although the claims have not been rejected on that ground, the Examiner has also complained about the use of the term "relatively" in Claims 3, 9, 10, 11, 17 and 21, and he has also objected to the term "high voltage" in Claim 22.[1]

[1]Although the term "high voltage" was in Claim 22 as originally filed, the Examiner apparently failed to note that it was cancelled in the Amendment filed October 27, 2005.

Claims 1 - 13 and 15 - 18 have been rejected under 35 U.S. C. §103 as being unpatentable over Hsu et al. (U.S. 6,911,690) in view of Sakui et al. (U.S. 6,411,548) and Chapman et al. (U.S. 6,118,161). [2]

GROUPING OF CLAIMS

It is not acceptable to applicant to have the claims stand or fall together within the group in which they have been rejected. Different claims include different limitations, and the Board could very well find that at least some of the claims are directed to patentable subject matter even if it were to affirm the Examiner's rejection of others.

ARGUMENT

35 U.S.C. §112 Rejections

Claims 19 - 22

In suggesting that the specification lacks support for the limitation calling for bit line diffusions and source diffusions spaced alternately in the active area with no other diffusions between themthe Examiner has apparently failed to recognize that the memory cells shown in the drawings are only part of an array having many groups of cells of the type illustrated. As illustrated, for example, in Figures 2 and 7 and described at Page 5, lines 6 - 12, each group is positioned between a bit line diffusion 50 and a source diffusion 51 which are common to the two groups of cells on either side of them. In that regard, it will be noted that Figures 2 and 7 each illustrate one complete group of cells, plus the beginning of the next group of cells on the other side of the common source 51, and this relationship is described at Page 6, lines 12 - 16 of the specification which read as follows:

> Select gates 44 and 45 partially overlap bit line diffusion 50 and common source diffusion 51, with edge portions of the two gates being positioned above edge portions of the diffusions. The diffusions extend continuously in a direction perpendicular to the rows in which the cells are grouped, and are shared by groups of cells on both sides of the diffusions.

From this disclosure, it should be quite clear to a person skilled in the art that the bit line diffusions and source diffusions are indeed spaced alternately in the active area with no other diffusions between them.

Claims 4, 18 and 22

The language to which the Examiner had objected is being cancelled. Hence, the rejection of Claims 4, 18 and 22 as being indefinite is now moot.

Claims 3, 9, 10, 11, 17 and 21

Since it appears that the Examiner may have intended to reject Claims 3, 9, 10, 11, 17 and 21 as being indefinite because of the use of the term "relatively", applicant will once again address the issue.

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[2] The Examiner apparently intended to include Claim 24 in this rejection since it is included in the discussion even though it is not included in the statement of the rejection.

In each of the claims in which the term "relatively" appears, it is not used by itself, but always in pairs to designate the comparative or relative sizes of two quantities, *e.g.* a "relatively thin" layer and a "relatively thick" one, a "relatively high" voltage and a "relatively low" one. Contrary to the Examiner's suggestion, this is not a case where one skilled in the art would not be apprised of the scope of the invention because the term "relatively" is not defined by the claims and the specification does not provide a standard for ascertaining the requisite degree. The term "relatively" is not being used to identify a particular quantity of level, but rather to define the comparative sizes of two quantities. Hence, for example, where a claim calls for a relatively thin oxide and a relatively thick oxide, a person skilled in the art is going to know that the claim simply requires the second oxide to be thicker than the first. Likewise, a claim calling for a relatively low voltage and a relatively high voltage simply requires the second voltage to be higher than the first. Thus, when the claims are considered in their entirety, there is no ambiguity.

Claim 22

In continuing to object to the term "high voltage" in Claim 22, the Examiner has apparently overlooked the fact that the term is no longer in the claim, and the point is moot.

35 U.S.C. § 103 Rejections

In rejecting Claims 1 - 13, 15 - 18, and presumably also Claim 24 under 35 U.S.C. §103 as being unpatentable over Hsu et al. in view of Sakui et al. and Chapman et al., the Examiner has misconstrued and mischaracterized what is actually found in the references and has tried to combine selected elements from the different references when there is no basis for doing so.

The array shown in Hsu et al. has a string of memory cell structures 132a - 132d formed between drain and source regions 124, 126. There are no bit lines, bit line diffusions or bit line contacts, as in applicant's invention, nor is there any overlapping or partial overlapping of a source region by a select gate.

In an attempt to create a bit line diffusion where none exists, the Examiner first mischaracterizes drain region 124 of Hsu et al. as a bit line diffusion, then later makes the illogical, unsupported and totally specious argument that a bit line diffusion inherently is contacted with a bit line and that both a bit line and a bit line contact must therefore exist. Notwithstanding the Examiner's efforts, the simple fact is that there are no bit line diffusions, no bit lines and no bit line contacts in Hsu et al.

Sakui et al. is cited as showing select gate - source region overlap in a NAND flash memory device. This rather obscure showing is found in Figure 49 of 72 figures in Sakui et al., with no motivation or other basis for combining it with the teachings of Hsu et al. and no suggestion as to how it might be done or what useful purpose it might serve. Moreover, the structure shown in Hsu et al. does not lend itself to having a select gate partially overlapping source region 126 because there is no select gate at that end of

the string of cells. Hence, adding a select gate and then having it partially overlap the source region is far beyond the teachings of the references.

Chapman et al. is cited as showing that for low series resistance and consistent high performance, it is well known that a gate should overlap with a source. However, that statement was made in the specific context of a MOSFET, not a NAND flash memory cell array, and there is no basis for the Examiner's contention that the select gate in any NAND flash memory device is no different from and ordinary gate in any transistor.

Claim 1 distinguishes over the combined teachings of the references in calling for a bit line diffusion and a source region in the active area of a substrate with no other diffusions in the active area between the bit line diffusion and the source region, a plurality of stacked gates and select gates arranged alternately in a row above the active area between the bit line diffusion and the source region, with each of the stacked gates having a control gate positioned above a floating gate and the last select gate in the row at least partially overlapping the source region, a bit line above the row, and a bit line contact interconnecting the bit line and the bit line diffusion. As discussed above, the references fail to teach or even suggest a bit line diffusion and a source region in the active area of a substrate with no other diffusions in the active area between the bit line diffusion and the source region. They likewise fail to show or suggest a row of stacked gates and select gates with the last select gate in the row at least partially overlapping the source region.

Claims 2 - 13 depend from Claim 1 and distinguish over the references for the same reasons as their parent claim. In addition, they call for additional features which are not found in or suggested by the references.

Claim 2 specifies that the stacked gates and the select gates are self-aligned relative to each other.

Claim 3 further distinguishes in calling for a relatively thin tunnel oxide between the floating gates and the substrate, a first relatively thick dielectric between the floating gates and the select gates, and a second relatively thick dielectric between the floating gates and the control gates. As the Examiner has acknowledged, this relationship is not taught by Hsu et al. or the other references. Hsu et al. is silent as to the relative thickness of the different dielectrics, and there is no basis for the Examiner's argument that cost considerations mandate that two of the dielectric layers should be thicker than the other.

Claim 4 further distinguishes in specifying that the control gates and the select gates surround the floating gates in a manner which provides inter-gate capacitances between the select gates and the floating gates and between the control gates and the floating gates which are large enough to couple voltages between the select gates and the floating gates and between the control gates and the floating gates. In arguing that any non-zero inter-gate capacitance implies a voltage coupling between the gates, the

Examiner has failed to consider the clear language of the claim which defines the control gates and the select gates as surrounding the floating gates.

Claim 5 further specifies that erase paths extend from the floating gates, through tunnel oxides below the floating gates to channel regions in the substrate, and voltage is coupled to the floating gates both from the control gates and from the select gates.

Claim 6 specifies that program paths extend from off-gate channel regions between the select gates and the floating gates to the floating gates, and voltage is coupled to the floating gates both from the control gates and from the select gates on the sides of the stacked gates toward the source region.

Claims 7 - 12 further distinguish over the references in calling for the application of specific voltages to different elements in the memory array.

In that regard, Claim 7 specifies that program paths extend from off-gate channel regions between the select gates and the floating gates to the floating gates, and the select gate on the bit line side of the stacked gates in a selected cell is biased at a lower voltage than the other select gates in the row to control channel current for efficient hot carrier injection during a program operation.

Claim 8 specifies that the select gates in unselected cells are biased at a voltage to turn on the channels beneath them to form a conduction path between the bit line diffusion and the source region. Here again, the Examiner has erred in ignoring a specific structural limitation as to the manner in which specific elements are biased. The intended use or functional language argument is the same one that the Examiner made in connection with the rejection of Claim 7, and it is fallacious for the same reasons.

Claim 9 specifies that the bit line for a row containing a selected cell to be programmed is held at 0 volts, a relatively low positive voltage is applied to a cell select gate for the selected cell, a relatively high positive voltage is applied to the source region at the end of the row in which the selected cell is located, a relatively high positive voltage is applied to the control gate in the selected cell, a relatively high positive voltage is applied to the select gates for unselected cells, and a relatively high positive voltage is applied to the control gates in the unselected cells. Here again, the Examiner has failed to give patentable weight to the specific limitations which distinguish over the references.

Claim 10 specifies that an erase path is formed by a relatively high negative voltage on the control gates and a relatively low negative voltage on the select gates, with the bit line diffusion, the source region and the P-well at 0 volts.

Claim 11 specifies that an erase path is formed by a relatively high negative voltage on the control gates, and a relatively low negative voltage on the select gates, with the active area at a positive voltage and the bit line diffusion and the source region floating.

Claim 12 specifies that a read path is formed by turning on the select transistors and the stacked control and floating gate transistors in unselected cells, with the common source at 0 volts, the bit line diffusion at 1 - 3 volts, and the control gate of the selected

cell biased at 0 – 1.5 volts to form a conduction channel under the floating gate for an erase state and a non-conduction channel for a program state.

The Examiner has taken the position that biasing and the application of other voltages are "intended use" or functional limitations to which no patentable weight is given. In so doing, he has overlooked the fact that the biasing of a specific element in a specific manner relative to other specific elements in a specific operational mode and the application of specific and/or relative voltages to specific elements are indeed structural limitations. Although they may define the structure as it is in use, they are nevertheless structural in nature and, therefore, entitled to patentable weight.

Claim 13 further calls for an erase path which can erase the whole cell array simultaneously and a program path which is single cell selectable.

Claim 15 distinguishes over the references in calling for a bit line diffusion and a source diffusion in the active area of a substrate with no other diffusions in the active area between the bit line diffusion and the source diffusion, a plurality of stacked gates and select gates arranged alternately in a row above the active area between the bit line diffusion and the source diffusion, with each of the stacked gates having a control gate positioned above a floating gate and the last select gate in the row being directly above the source diffusion, a bit line above the row, and a bit line contact interconnecting the bit line and the bit line diffusion. As noted above, the references fail to teach or even suggest a bit line diffusion and a source region in the active area of a substrate with no other diffusions in the active area between the bit line diffusion and the source region. They likewise fail to show or suggest a row of stacked gates and select gates with the last select gate in the row being directly above the source region. , and the Examiner is mistaken in suggesting that this structure is shown in Sakui et al.

Claims 16 - 18 depend from Claim 15 and distinguish over the references for the same reasons as their parent claim. In addition, they call for additional features which are not found in or suggested by the references.

Claim 16 specifies that the select gates are self-aligned to the control and floating gates.

Claim 17, like Claim 3, further distinguishes in calling for a relatively thin tunnel oxide between the floating gates and the substrate, a first relatively thick dielectric between the floating gates and the select gates, and a second relatively thick dielectric between floating gates and control gates.

Claim 18, like Claim 4, further distinguishes in specifying that the control gates and the select gates surround the floating gates in a manner which provides inter-gate capacitances between the select gates and the floating gates and between the control gates and the floating gates which are large enough to couple voltages between the select gates and the floating gates and between the control gates and the floating gates.

Claim 24 distinguishes over the references in calling for a bit line diffusion and a source region in the active area of a substrate with no other diffusions in the active

area between the bit line diffusion and the source region, a plurality of stacked gates and select gates arranged alternately in a row above the active area between the bit line diffusion and the source region, with each of the stacked gates having a control gate and a floating gate with self-aligned sides adjacent to the select gates, erase paths between the floating gates and channel regions in the active area beneath the stacked gates, and voltage coupling from the control gates and the select gates to the floating gates.

SUMMARY AND CONCLUSION

It is respectfully submitted that the rejections which the Examiner has made cannot be sustained and that the action of the Examiner should be reversed.

DEPOSIT ACCOUNT AUTHORIZATION

The Commissioner is authorized to charge any fees required in this matter, including extension fees to Deposit Account 50-2975, Order No. A-75000.

Respectfully submitted,

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CERTIFICATE OF FACSIMILE TRANSMISSION

I CERTIFY THAT THIS BRIEF ON APPEAL IS BEING FORWARDED TO THE PATENT OFFICE FOR FILING VIA FACSIMILE TRANSMISSION TO (571) 273-8300 ON July 10, 2006.

EDWARD S. WRIGHT

The Claims on Appeal

1. A NAND flash memory cell array, comprising: a substrate having an active area, a bit line diffusion and a source region in the active area with no other diffusions in the active area between the bit line diffusion and the source region, a plurality of stacked gates and select gates arranged alternately in a row above the active area between the bit line diffusion and the source region, with each of the stacked gates having a control gate positioned above a floating gate and the last select gate in the row at least partially overlapping the source region, a bit line above the row, and a bit line contact interconnecting the bit line and the bit line diffusion.

2. The memory cell array of Claim 1 wherein the stacked gates and the select gates are self-aligned relative to each other.

3. The memory cell array of Claim 1 including a relatively thin tunnel oxide between the floating gates and the substrate, a first relatively thick dielectric between the floating gates and the select gates, and a second relatively thick dielectric between the floating gates and the control gates.

4. The memory cell array of Claimwherein the control gates and the select gates surround the floating gates in a manner which provides inter-gate capacitances between the select gates and the floating gates and between the control gates and the floating gates which are large enough to couple voltages between the select gates and the floating gates and between the control gates and the floating gates.

5. The memory cell array of Claim 1 wherein erase paths extend from the floating gates, through tunnel oxides below the floating gates to channel regions in the substrate, and voltage is coupled to the floating gates both from the control gates and from the select gates.

6. The memory cell array of Claim 1 wherein program paths extend from off-gate channel regions between the select gates and the floating gates to the floating gates, and voltage is coupled to the floating gates both from the control gates and from the select gates on the sides of the stacked gates toward the source region.

7. The memory cell array of Claim 1 wherein program paths extend from off-gate channel regions between the select gates and the floating gates to the floating gates, and the select gate on the bit line side of the stacked gates in a selected cell is biased at a lower voltage than the other select gates in the row to control channel current for efficient hot carrier injection during a program operation.

8. The memory cell array of Claim 1 wherein the select gates in unselected cells are biased at a voltage to turn on the channels beneath them to form a conduction path between the bit line diffusion and the source region.

9. The memory cell array of Claim 1 wherein the bit line for a row containing a selected cell to be programmed is held at 0 volts, a relatively low positive voltage is applied to a cell select gate for the selected cell, a relatively high positive voltage is applied to the source region at the end of the row in which the selected cell is located, a relatively high positive voltage is applied to the control gate in the selected cell, a relatively high positive voltage is applied to the select gates for unselected cells, and a relatively high positive voltage is applied to the control gates in the unselected cells.

10. The memory cell array of Claim 1 wherein an erase path is formed by a relatively high negative voltage on the control gates and a relatively low negative voltage on the select gates, with the bit line diffusion, the source region and the P-well at 0 volts.

11. The memory cell array of Claim 1 wherein an erase path is formed by a relatively high negative voltage on the control gates, and relatively low negative voltage on the select gates, with the active area at a positive voltage and the bit line diffusion and the source region floating.

12. The memory cell array of Claim 1 wherein a read path is formed by turning on the select transistors and the stacked control and floating gate transistors in unselected cells, with the common source at 0 volts, the bit line diffusion at 1 - 3 volts, and the control gate of the selected cell biased at 0 – 1.5 volts to form a conduction channel under the floating gate for an erase state and a non-conduction channel for a program state.

13. The memory cell array of Claim 1 including an erase path which can erase the whole cell array simultaneously and a program path which is single cell selectable.

15. A NAND flash memory cell array, comprising: a substrate having an active area, a bit line diffusion and a source diffusion in the active area with no other diffusions in the active area between the bit line diffusion and the source diffusion, a plurality of stacked gates and select gates arranged alternately in a row above the active area between the bit line diffusion and the source diffusion, with each of the stacked gates having a control gate positioned above a floating gate and the last select gate in the row being directly above the source diffusion, a bit line above the row, and a bit line contact interconnecting the bit line and the bit line diffusion.

16. The memory cell array of Claim 15 wherein the select gates are self-aligned to the control and floating gates.

17. The memory cell array of Claim 15 including a relatively thin tunnel oxide between the floating gates and the substrate, a first relatively thick dielectric between the floating gates and the select gates, and a second relatively thick dielectric between floating gates and control gates.

18. The memory cell array of Claim 15 wherein the control gates and the select gates surround the floating gates in a manner which provides inter-gate capacitances between the select gates and the floating gates and between the control gates and the floating gates which are large enough to couple voltages between the select gates and the floating gates and between the control gates and the floating gates.

19. A NAND flash memory cell array, comprising: a substrate having an active area, bit line diffusions and source diffusions spaced alternately in the active area with no other diffusions between them, a plurality of stacked gates and select gates arranged alternately in rows between the bit line diffusions and the source diffusions, with each of the stacked gates having a control gate positioned above a floating gate and the last select gates in each of the rows at least partially overlapping the source diffusions between the rows, a bit line above each row, and bit line contacts interconnecting the bit lines and the bit line diffusions.

20. The memory cell array of Claim 19 wherein the floating gate and the control gate in each of the stacked gates are self-aligned with respect to each other.

21. The memory cell array of Claim 19 including a relatively thin tunnel oxide between the floating gates and the substrate, a first relatively thick dielectric between the floating gates and the select gates, and a second relatively thick dielectric between floating gates and control gates.

22. The memory cell array of Claim 19 wherein the control gates and the select gates surround the floating gates in a manner which provides inter-gate capacitances between the select gates and the floating gates and between the control gates and the floating gates which are large enough to couple voltages between the select gates and the floating gates and between the control gates and the floating gates.

24. A NAND flash memory cell array, comprising: a substrate having an active area, a bit line diffusion and a source region in the active area with no other diffusions in the active area between the bit line diffusion and the source region, a plurality of stacked gates and select gates arranged alternately in a row above the active area between the bit line diffusion and the source region, with each of the stacked gates having a control gate and a floating gate with self-aligned sides adjacent to the select gates, erase paths between the floating gates and channel regions in the active area beneath the stacked gates, and voltage coupling from the control gates and the select gates to the floating gates.